

FIG. 1

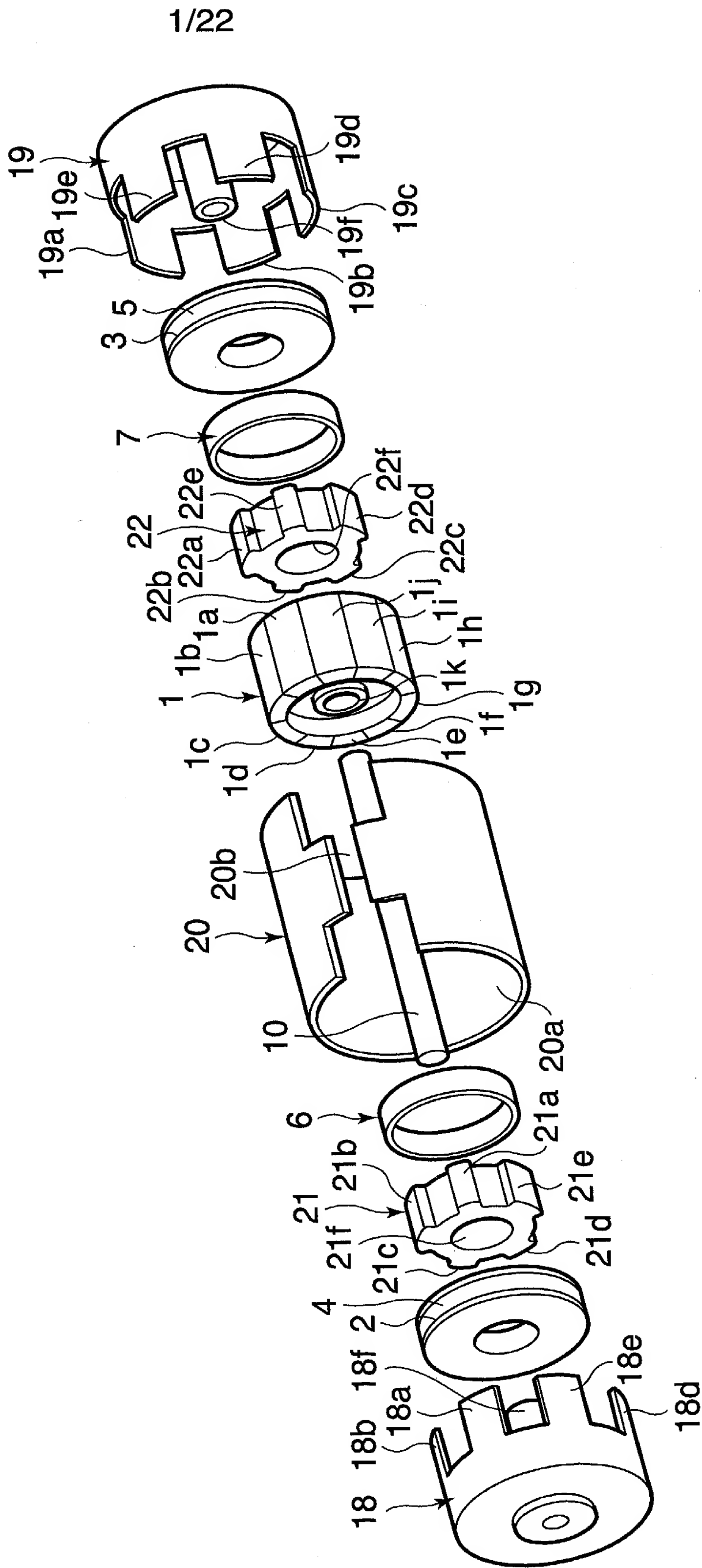
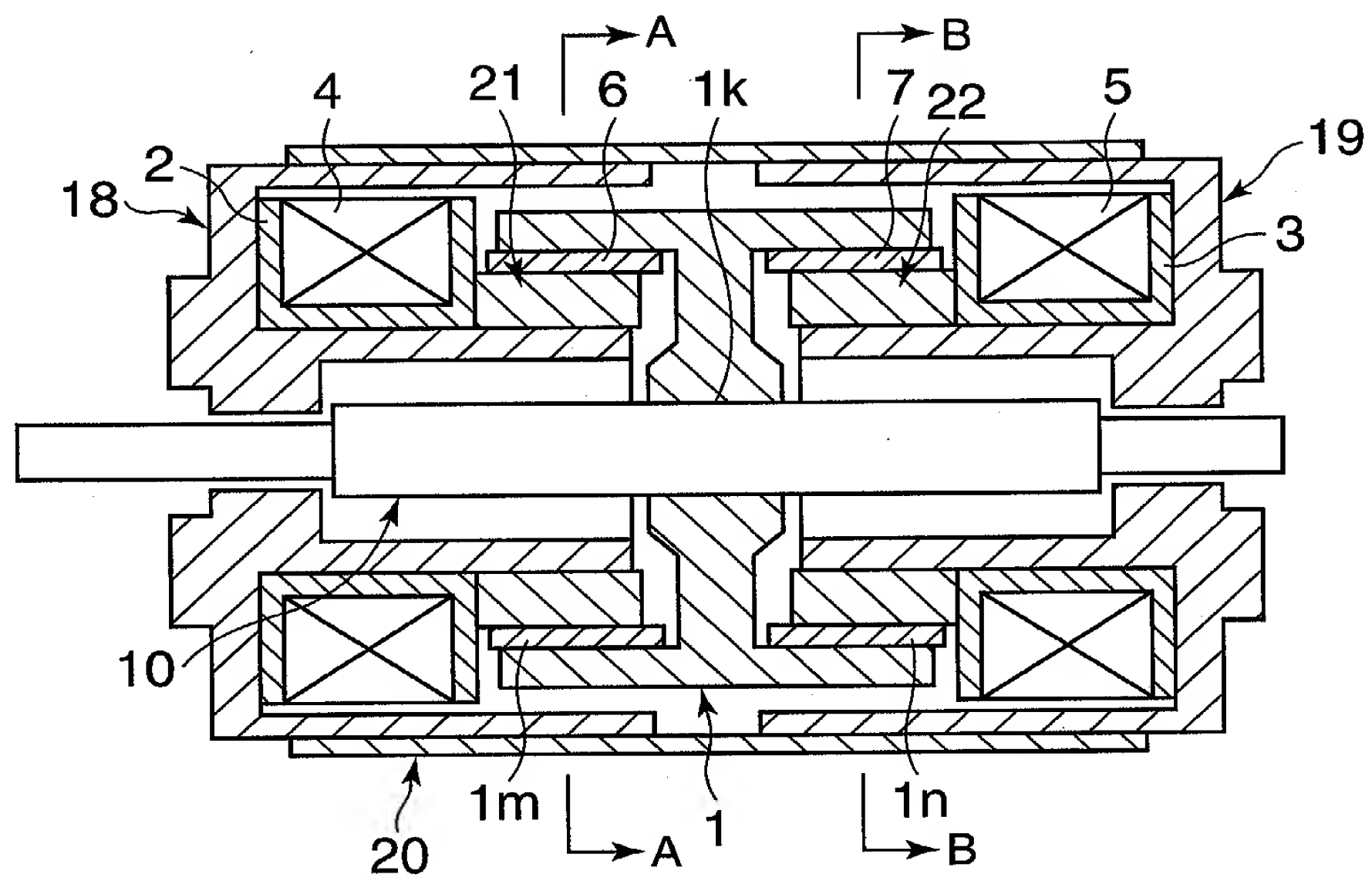


FIG.2



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FIG.3A

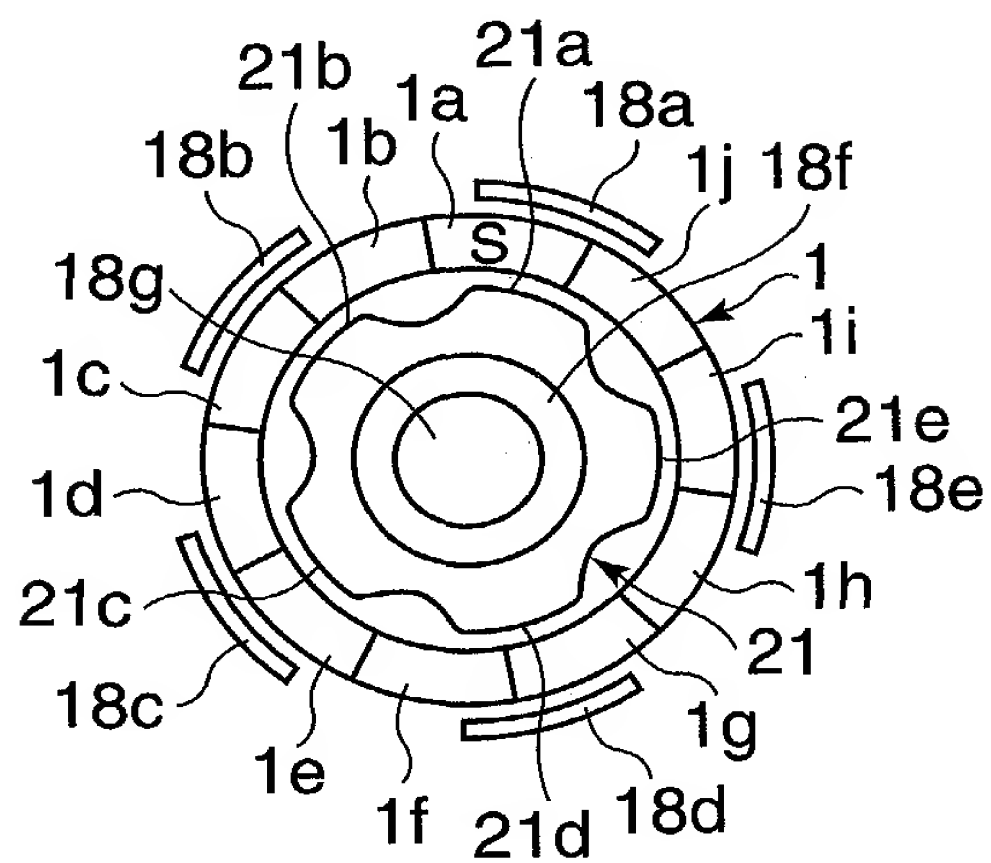


FIG.3B

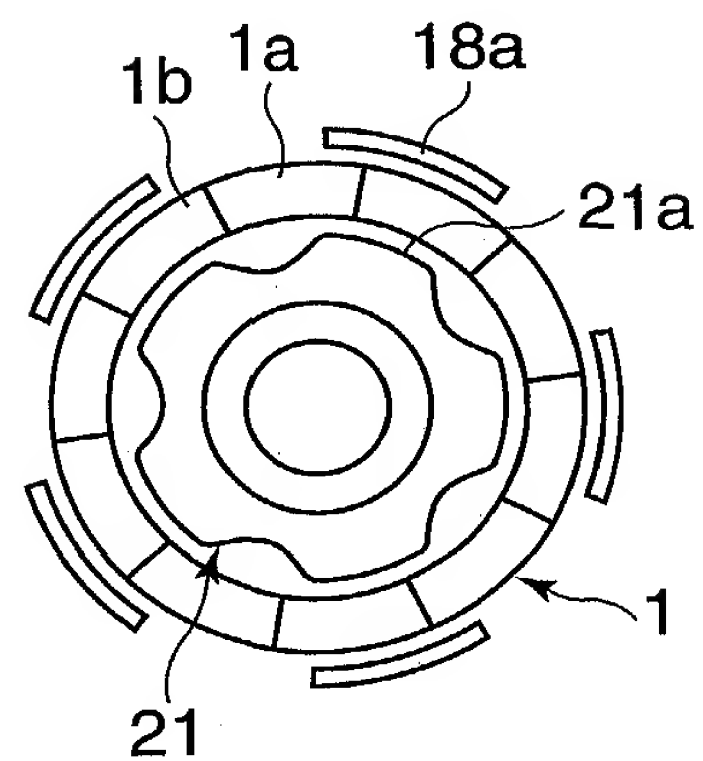


FIG.3C

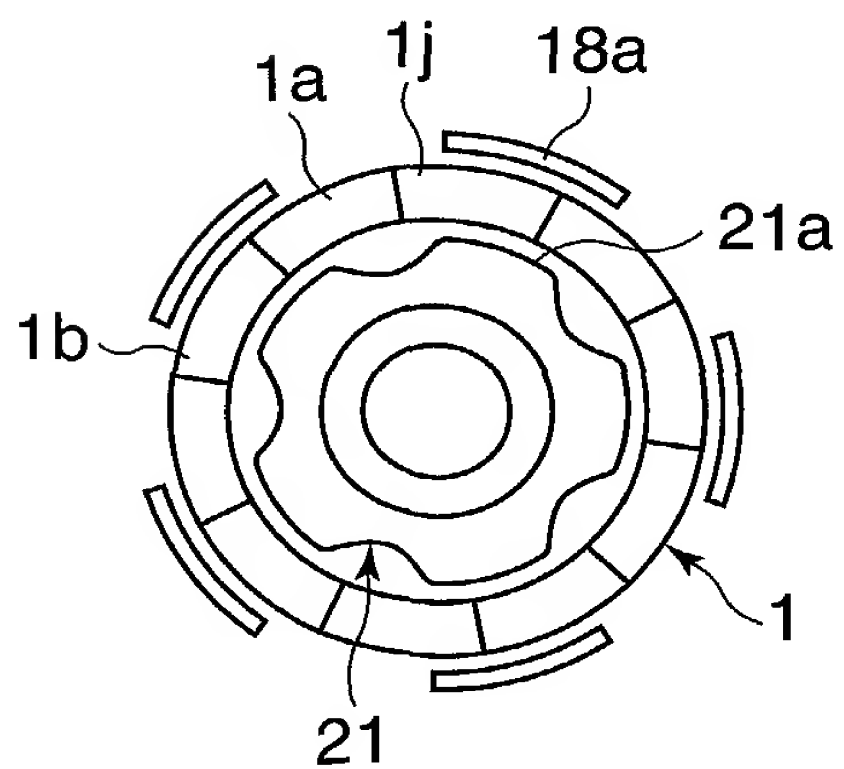


FIG.3D

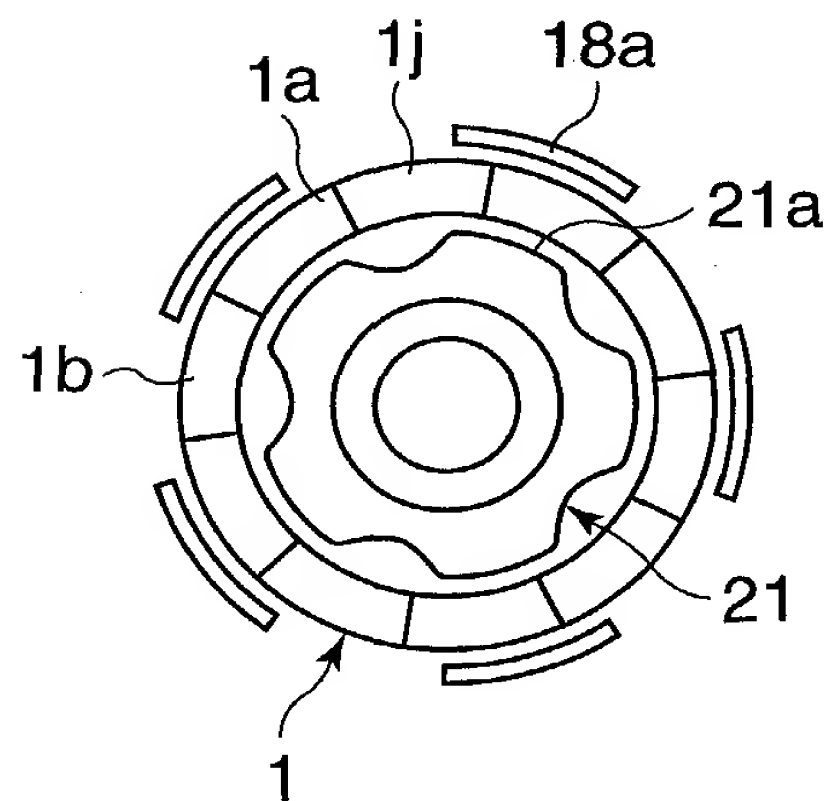


FIG.4A

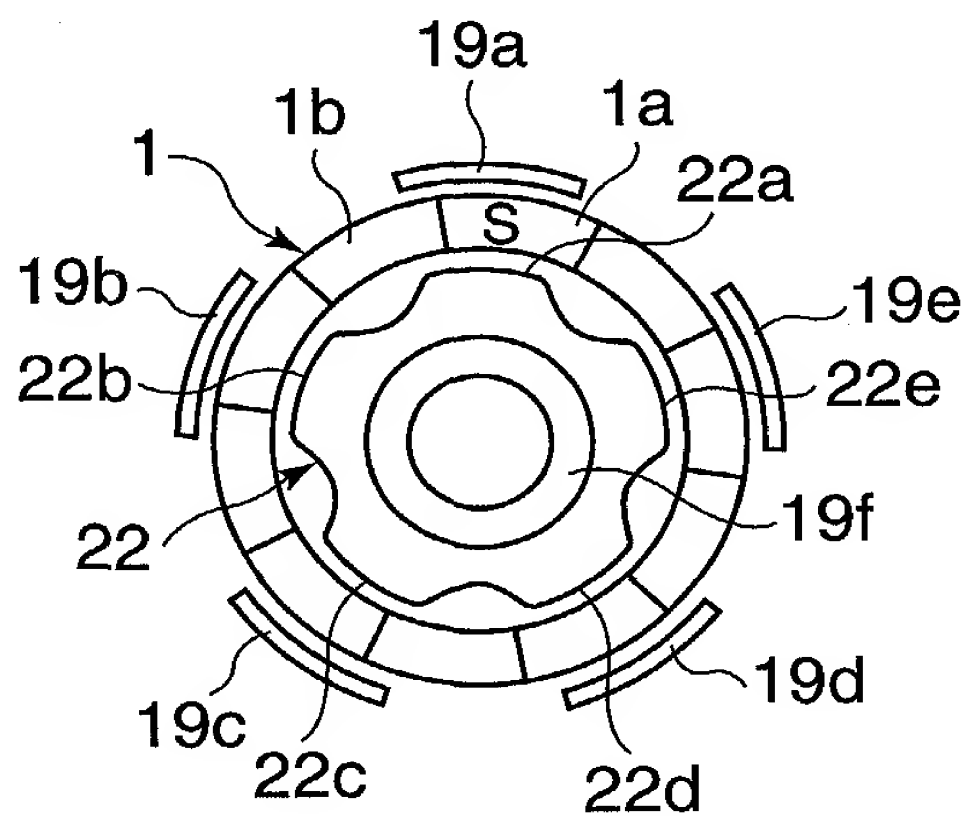


FIG.4B

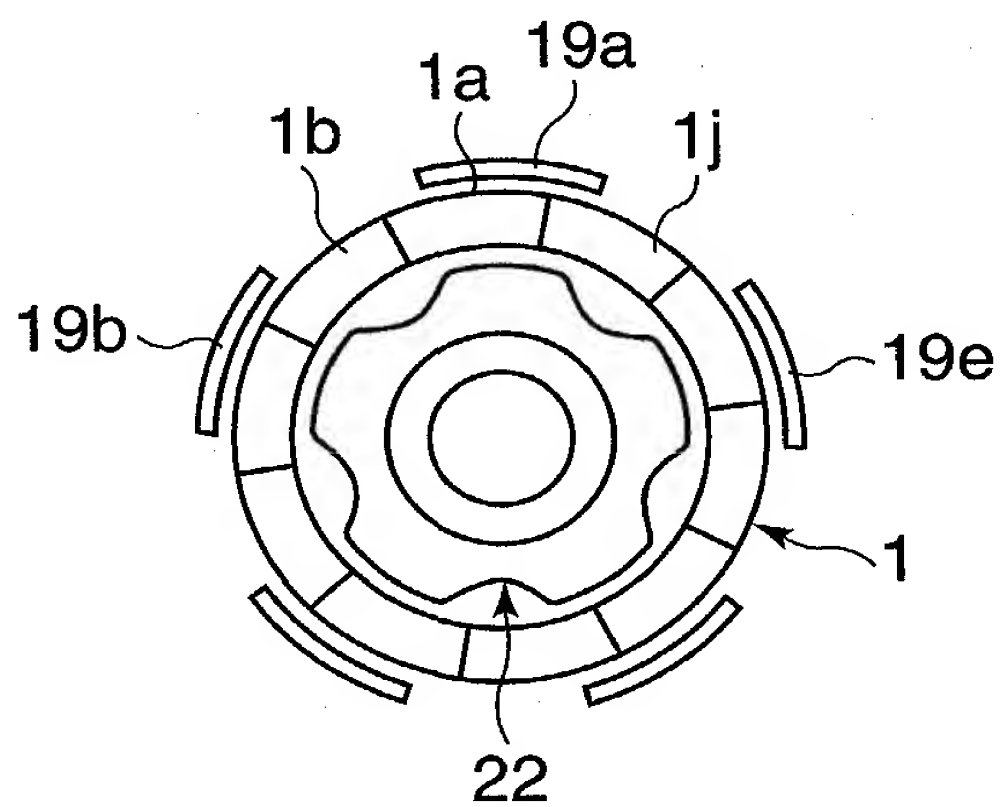


FIG.4C

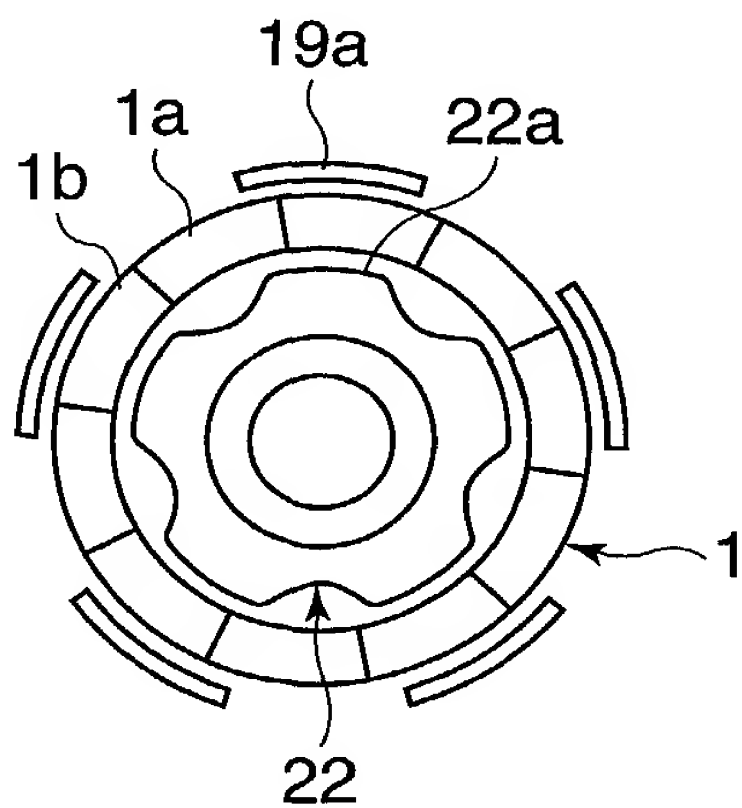
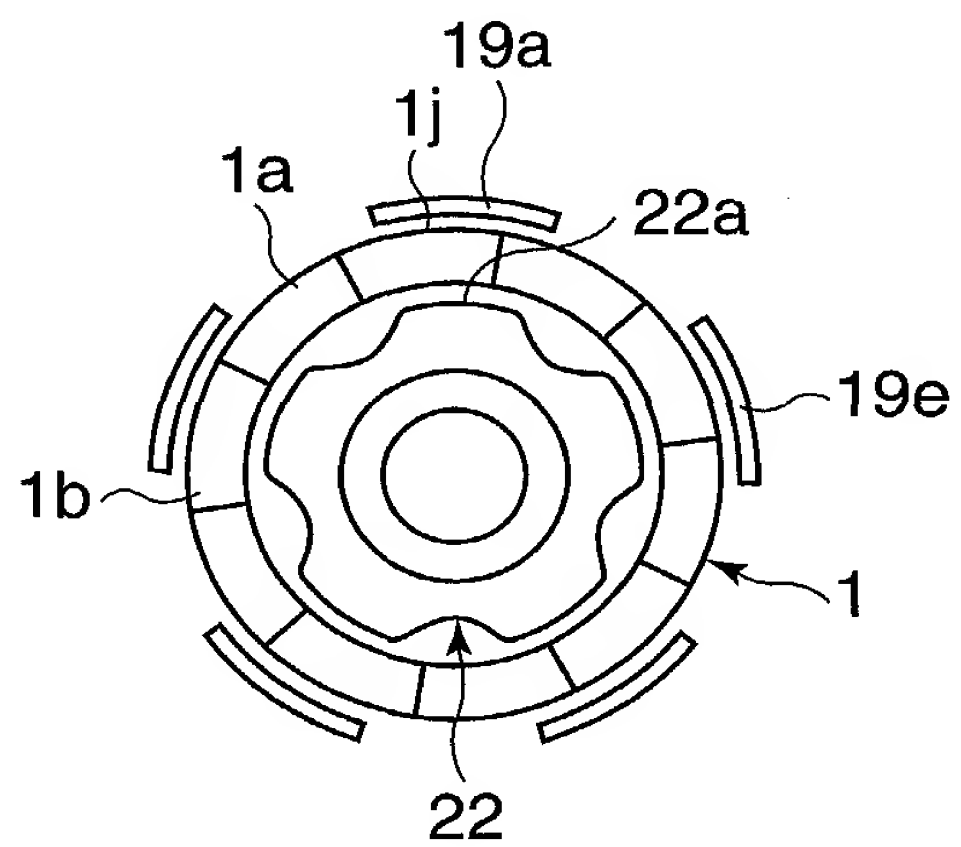


FIG.4D



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FIG.5

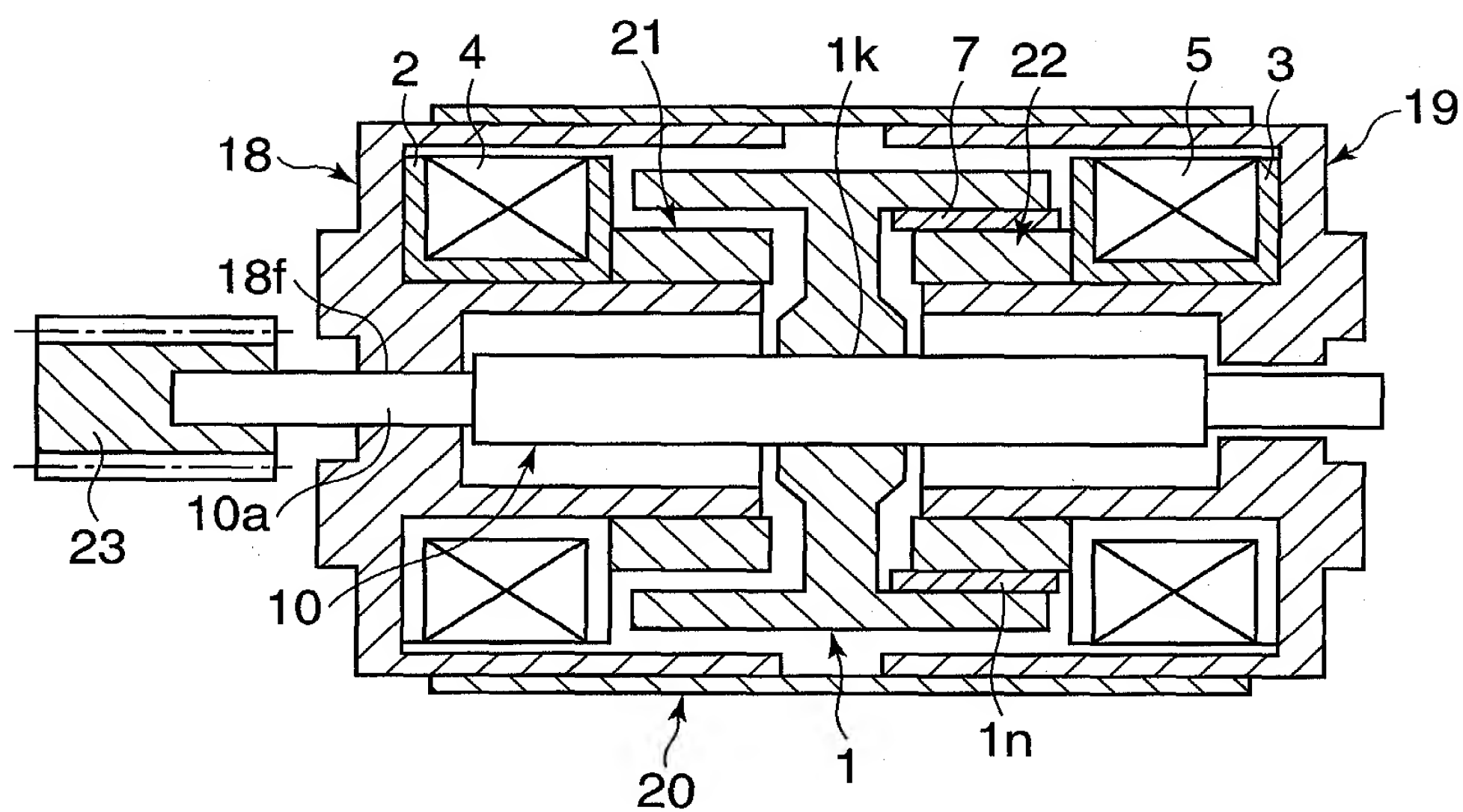
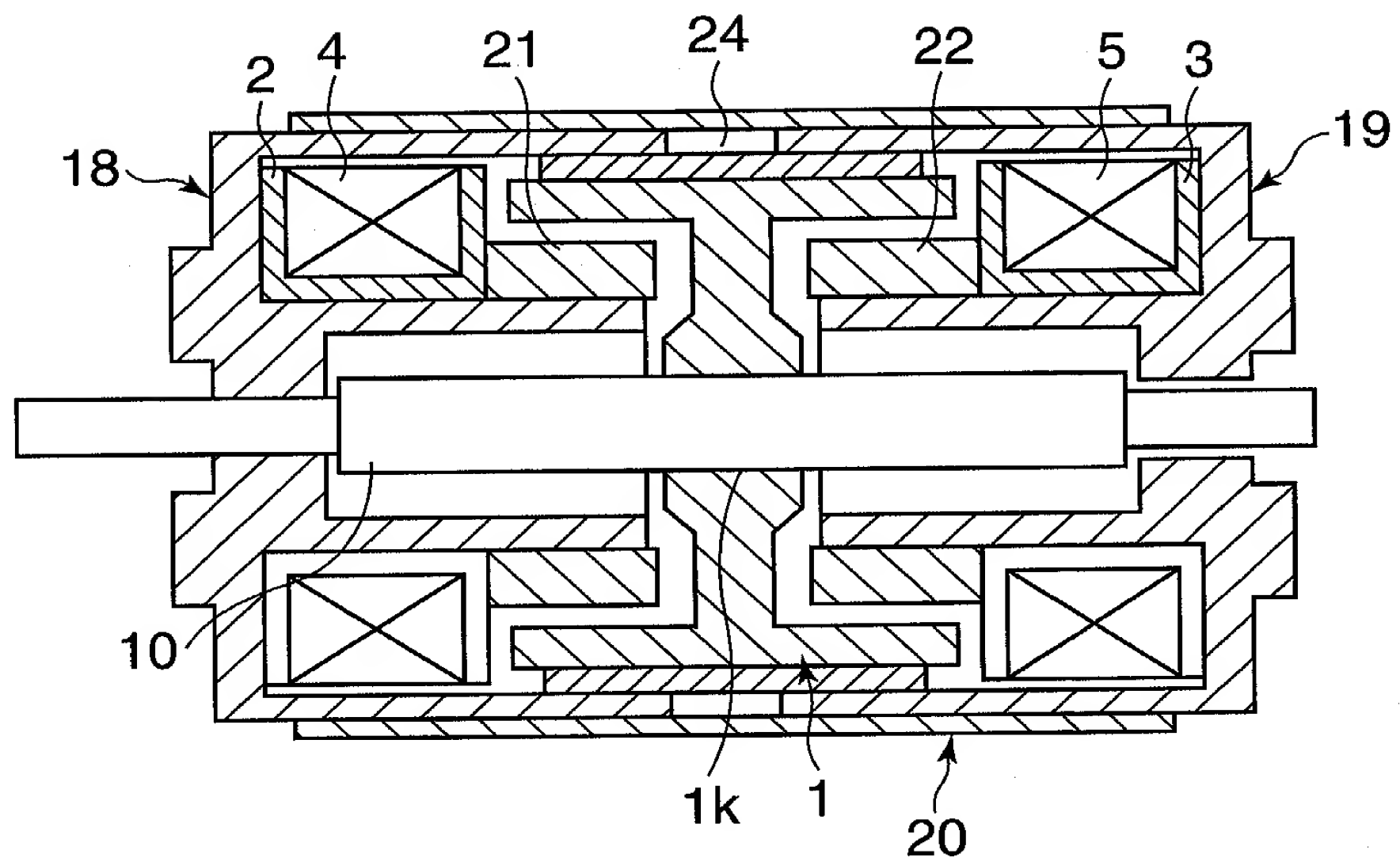


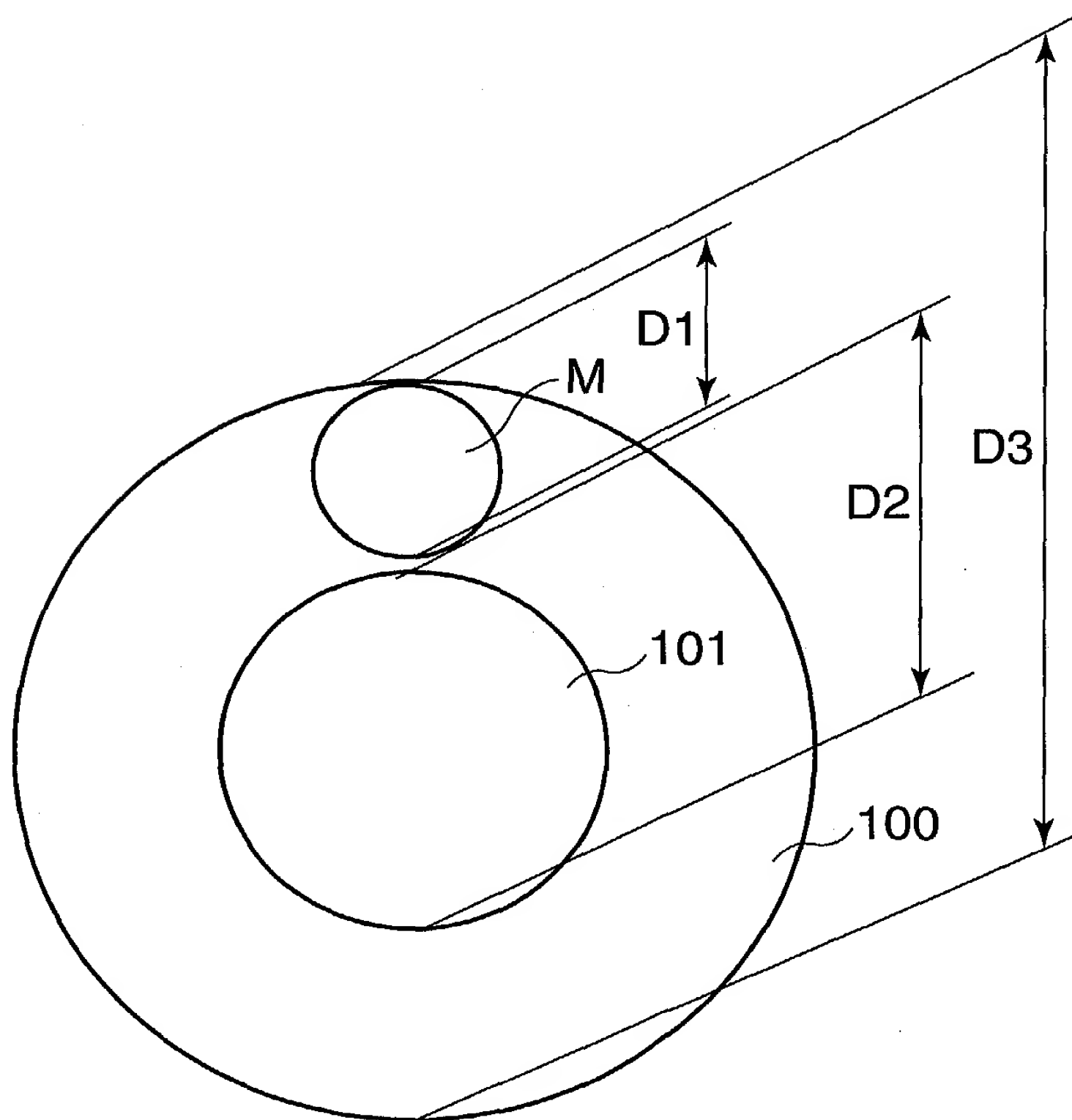
FIG.6



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00240-94001660

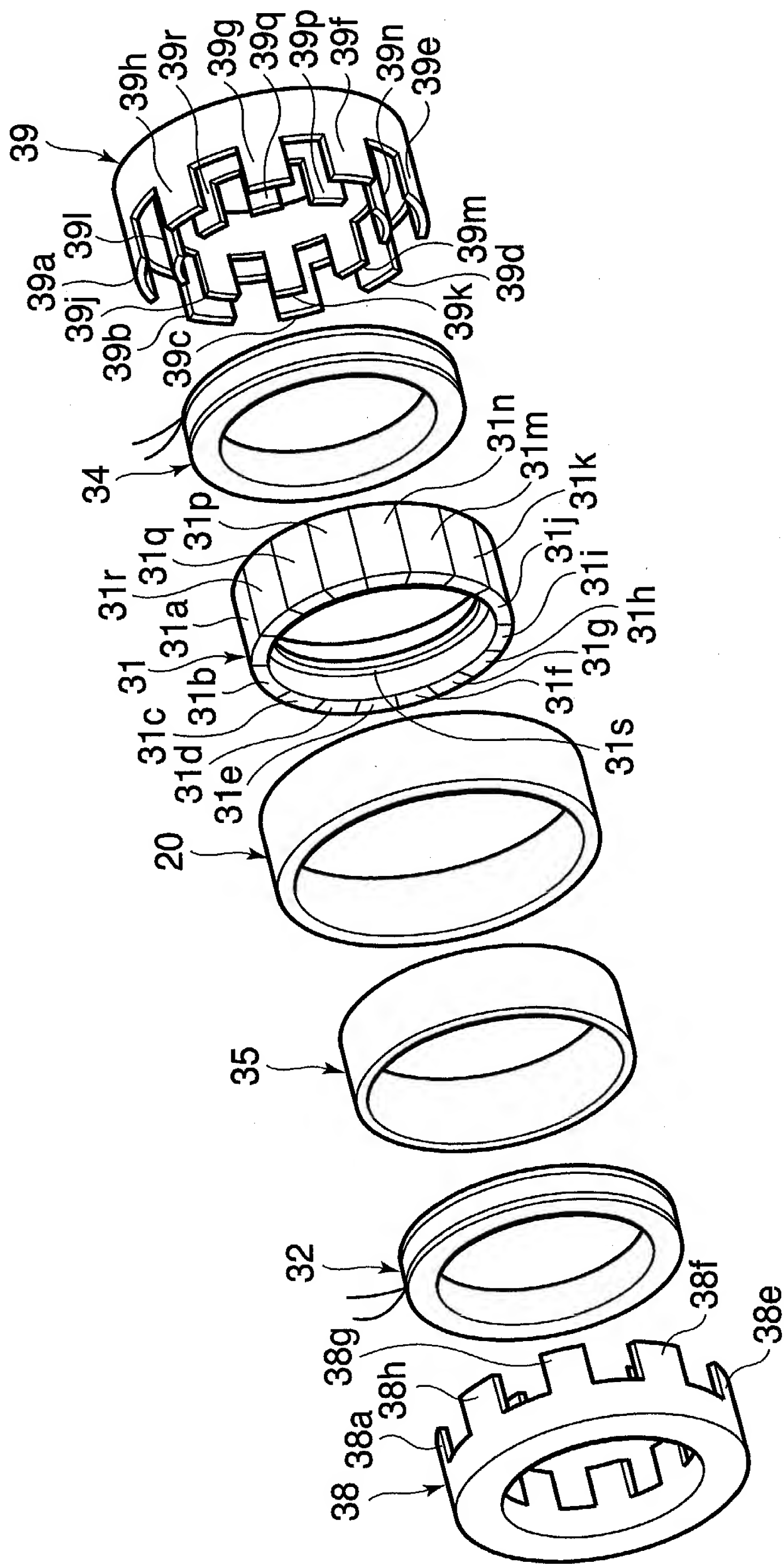
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FIG.7



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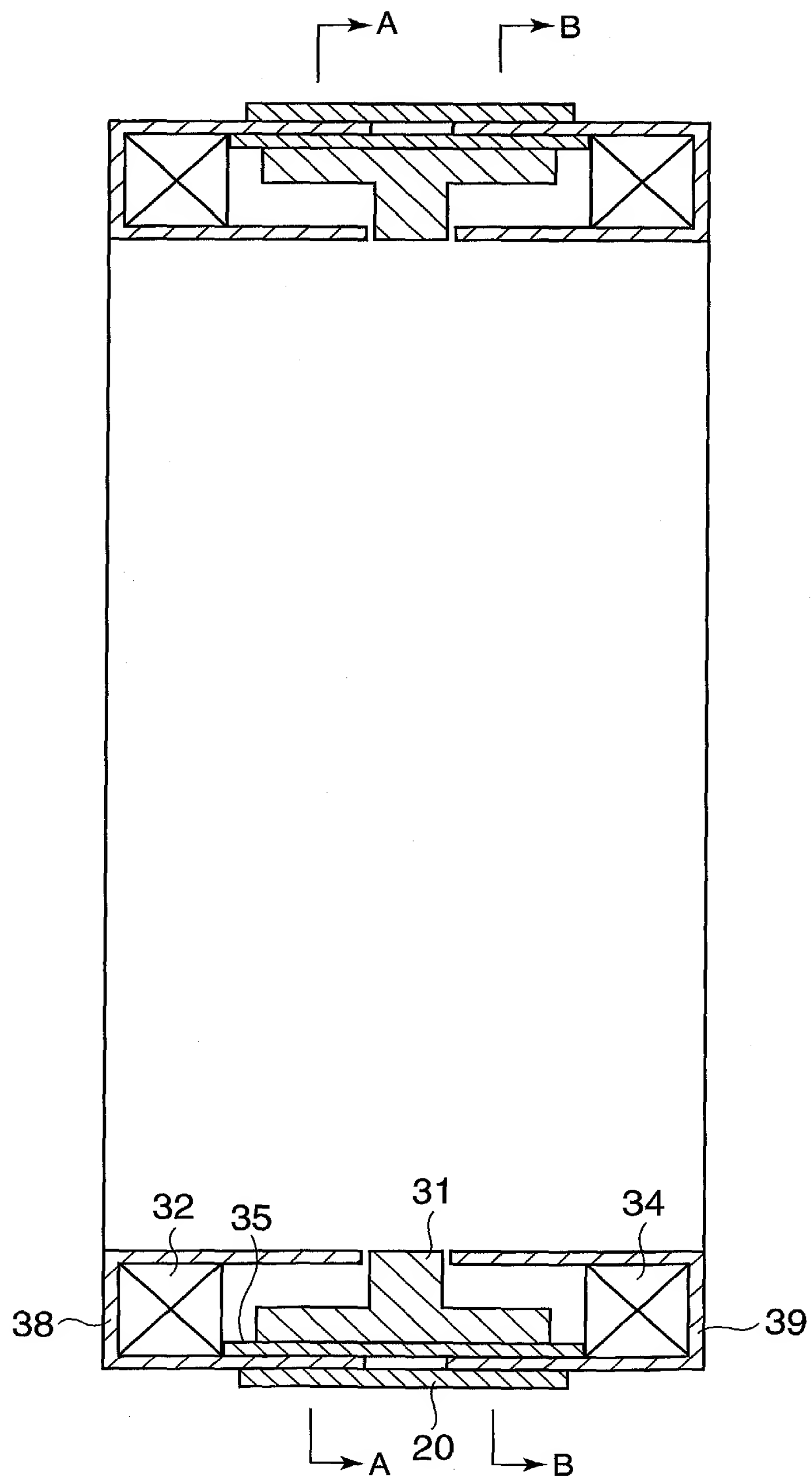
FIG. 8





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FIG.9



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FIG.10A

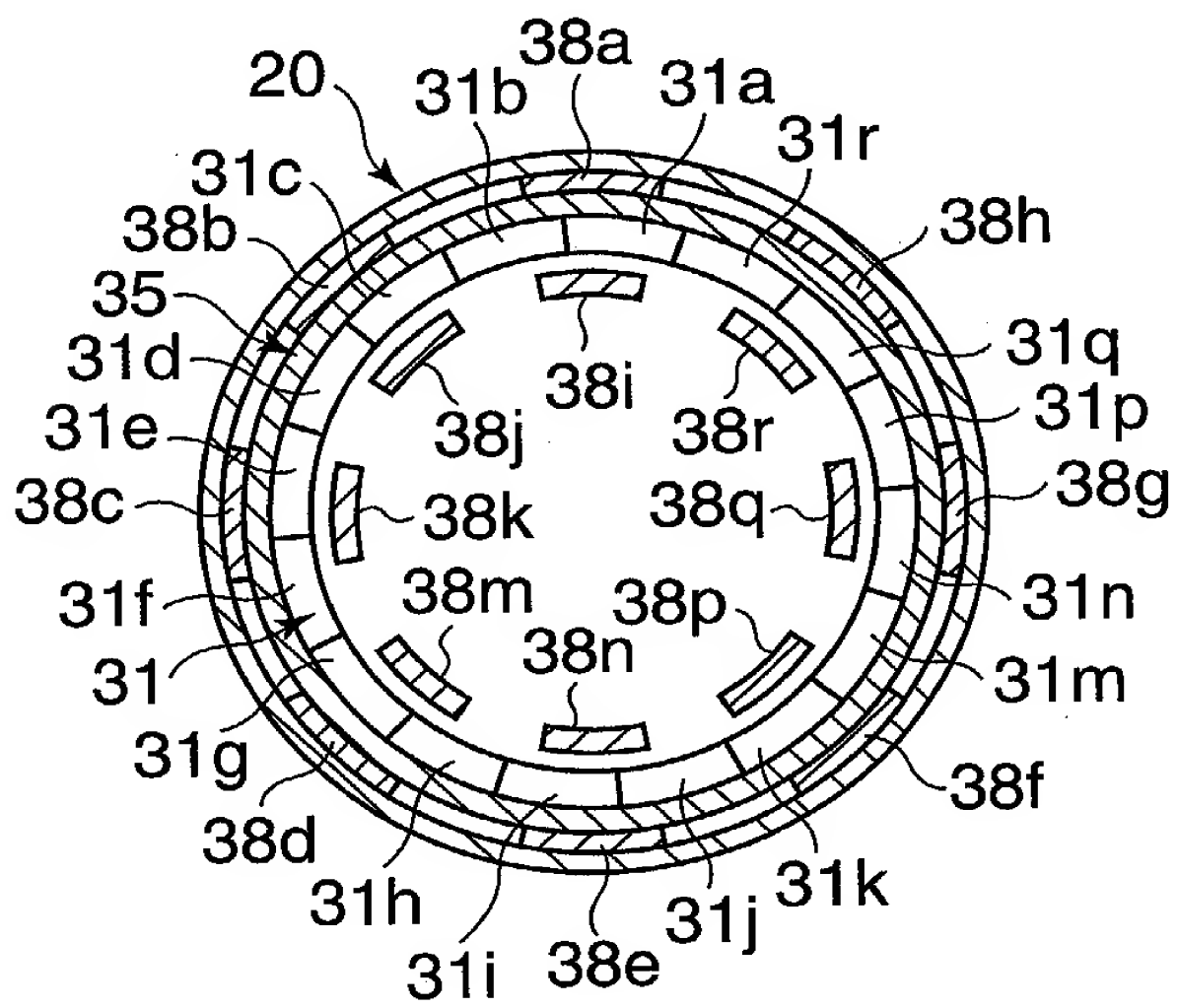


FIG.10B

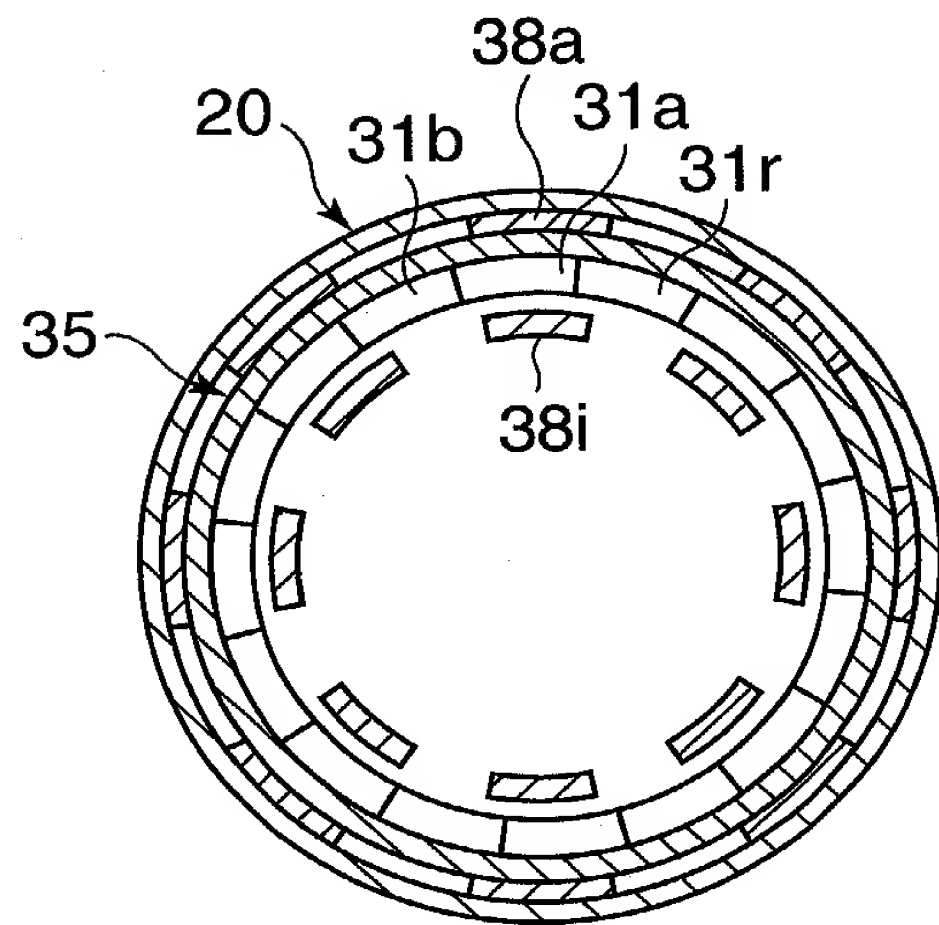


FIG.10C

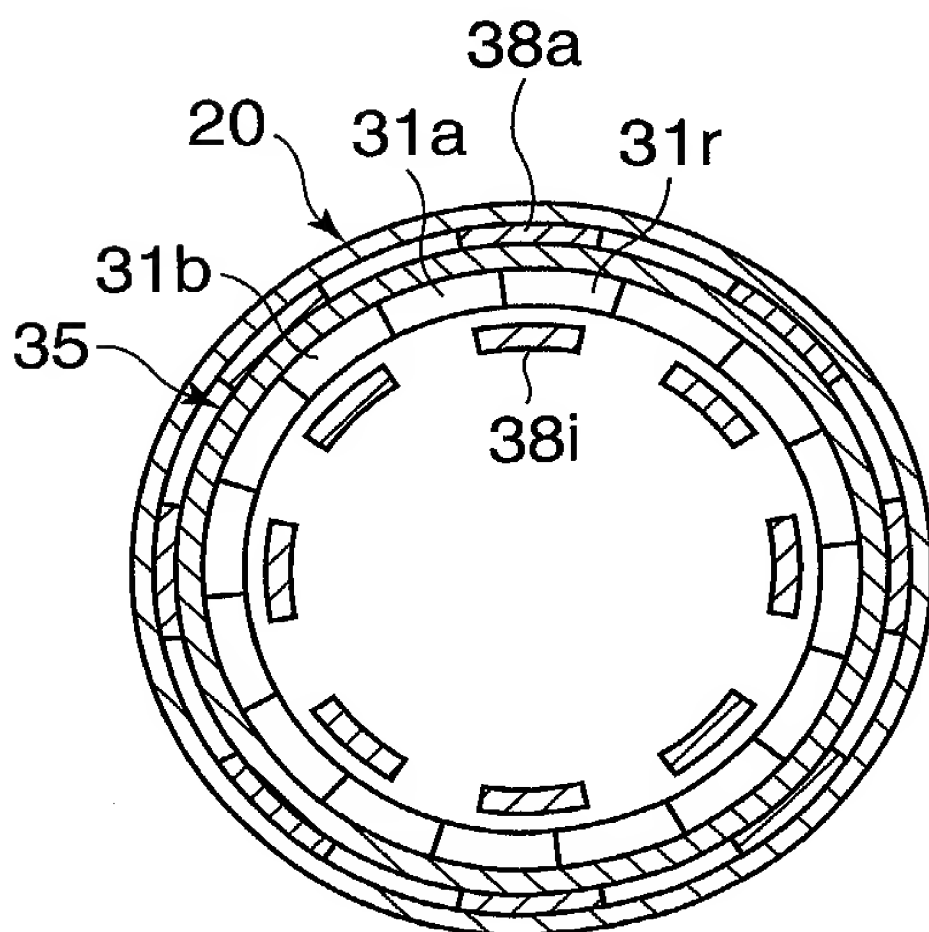


FIG.10D

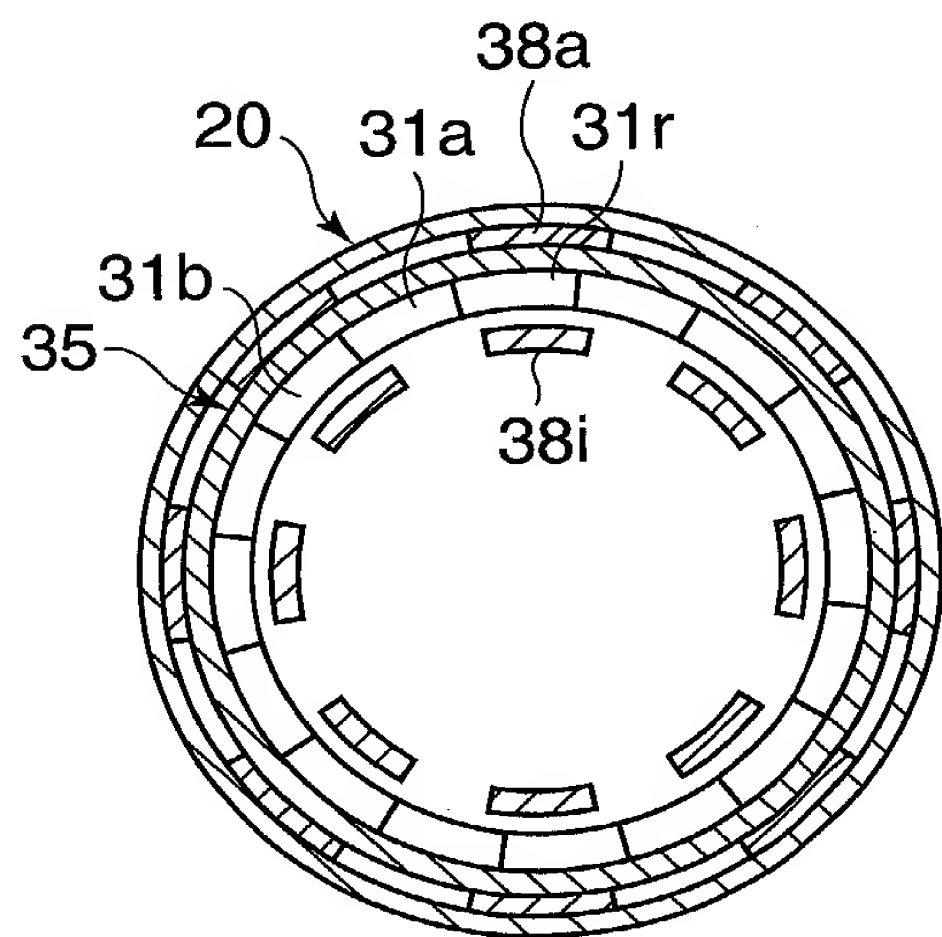


FIG.11A

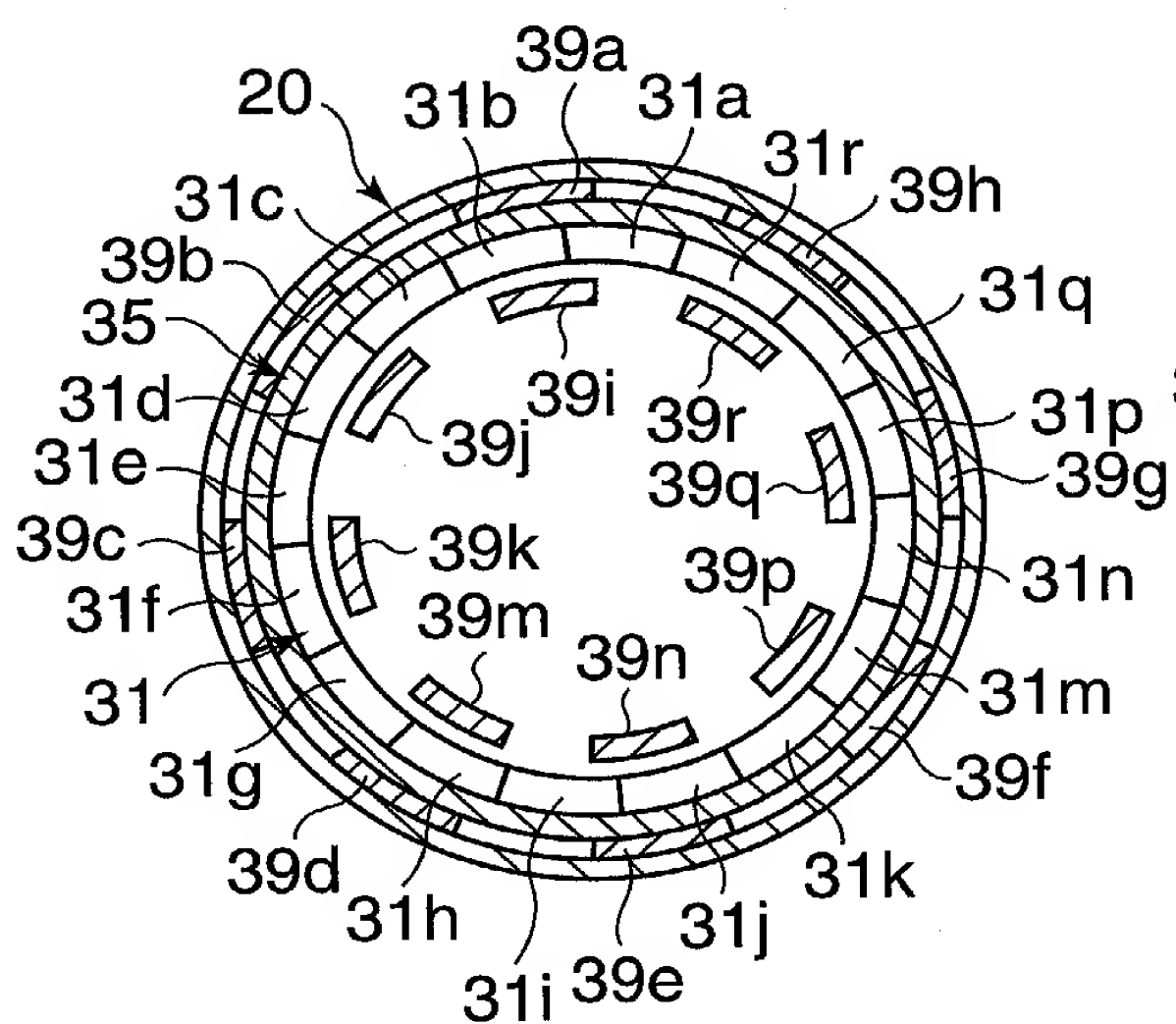


FIG.11B

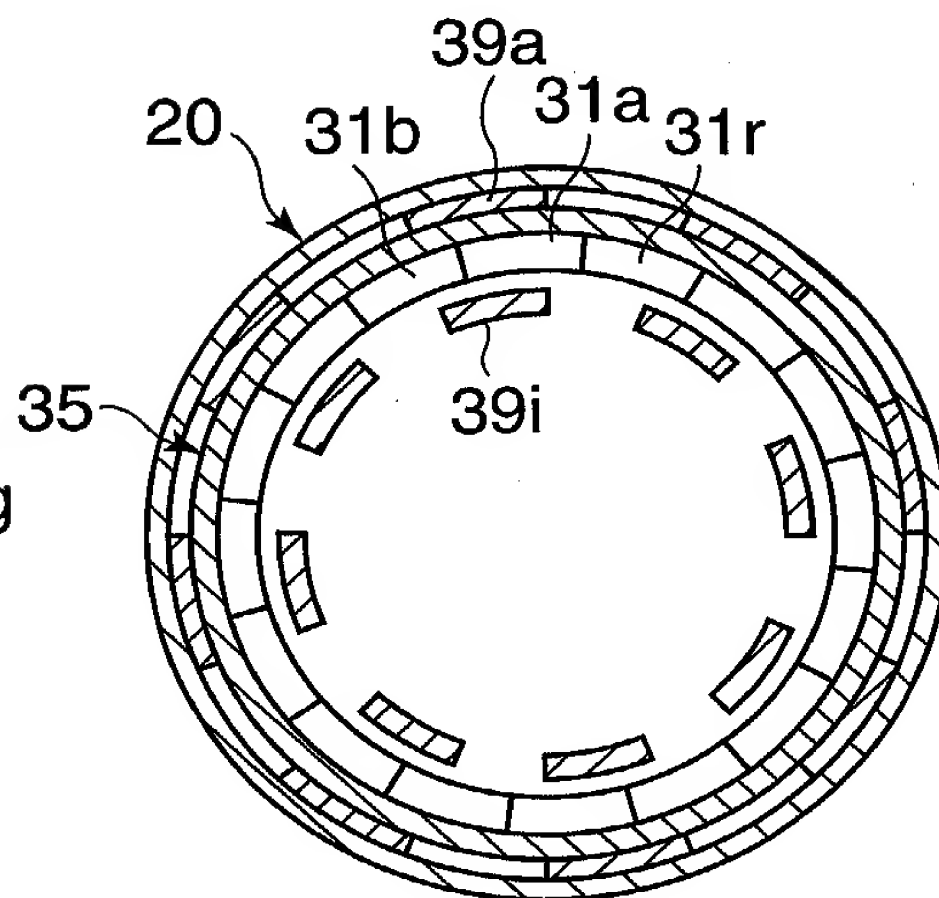


FIG.11C

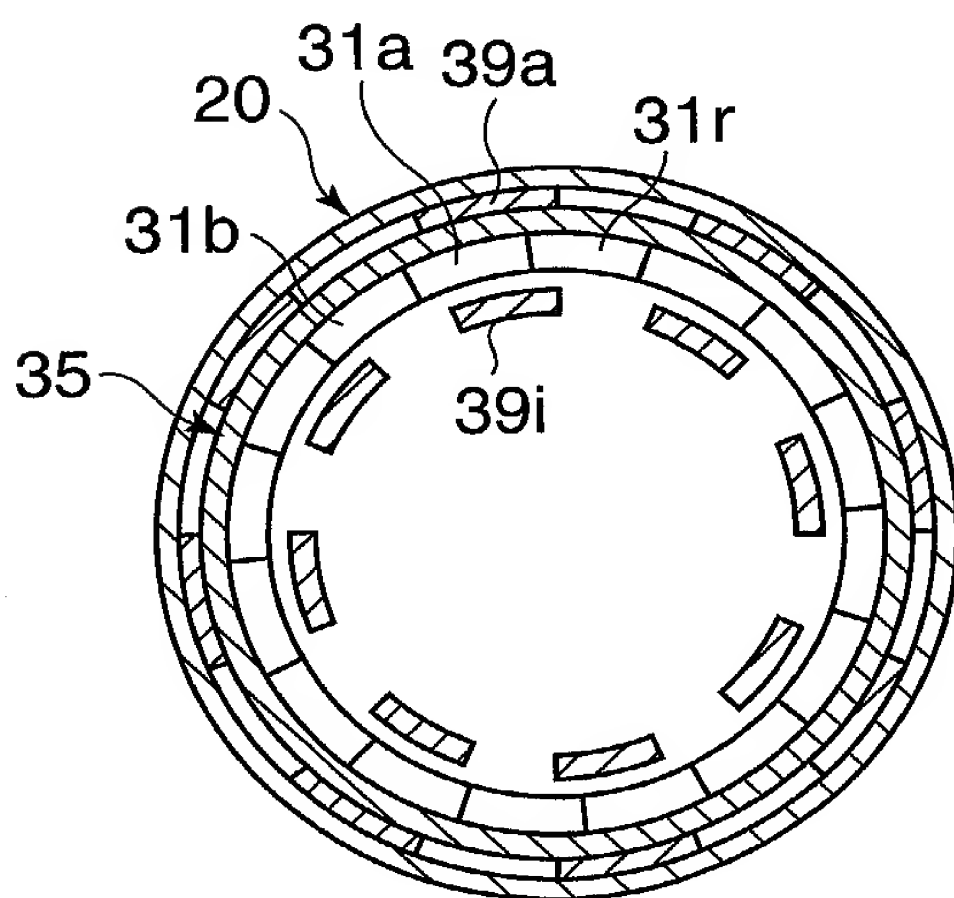
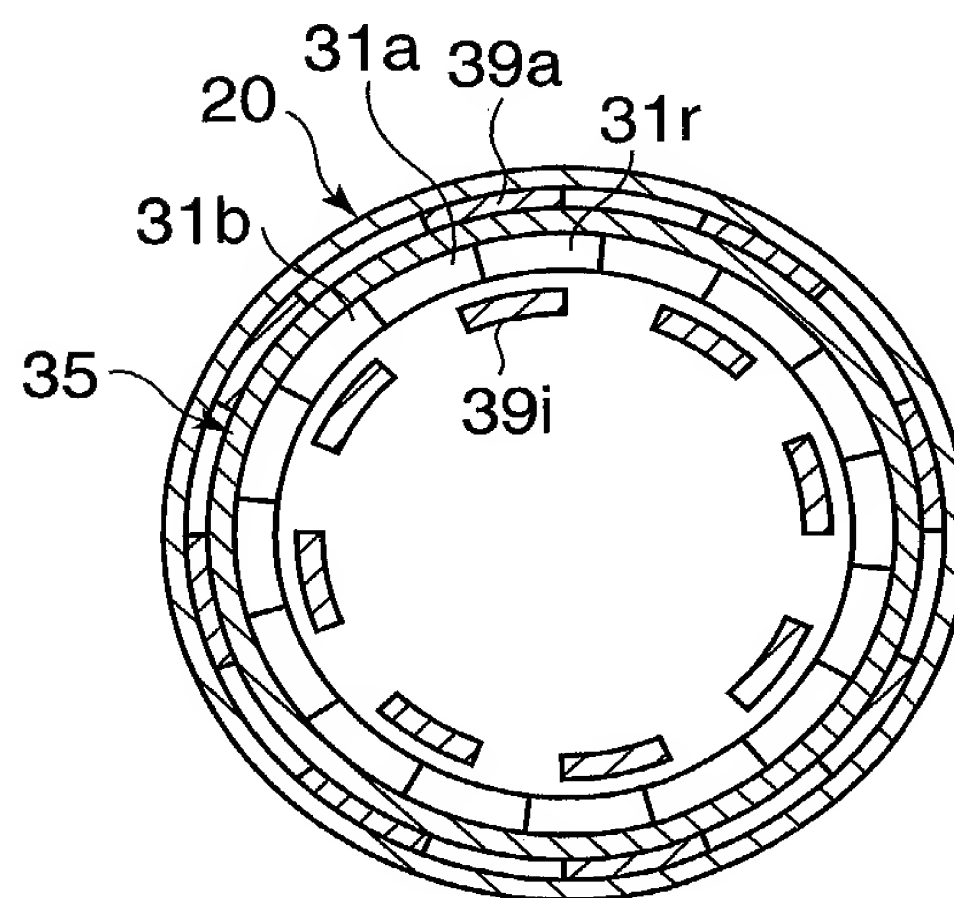


FIG.11D



**FIG. 12**

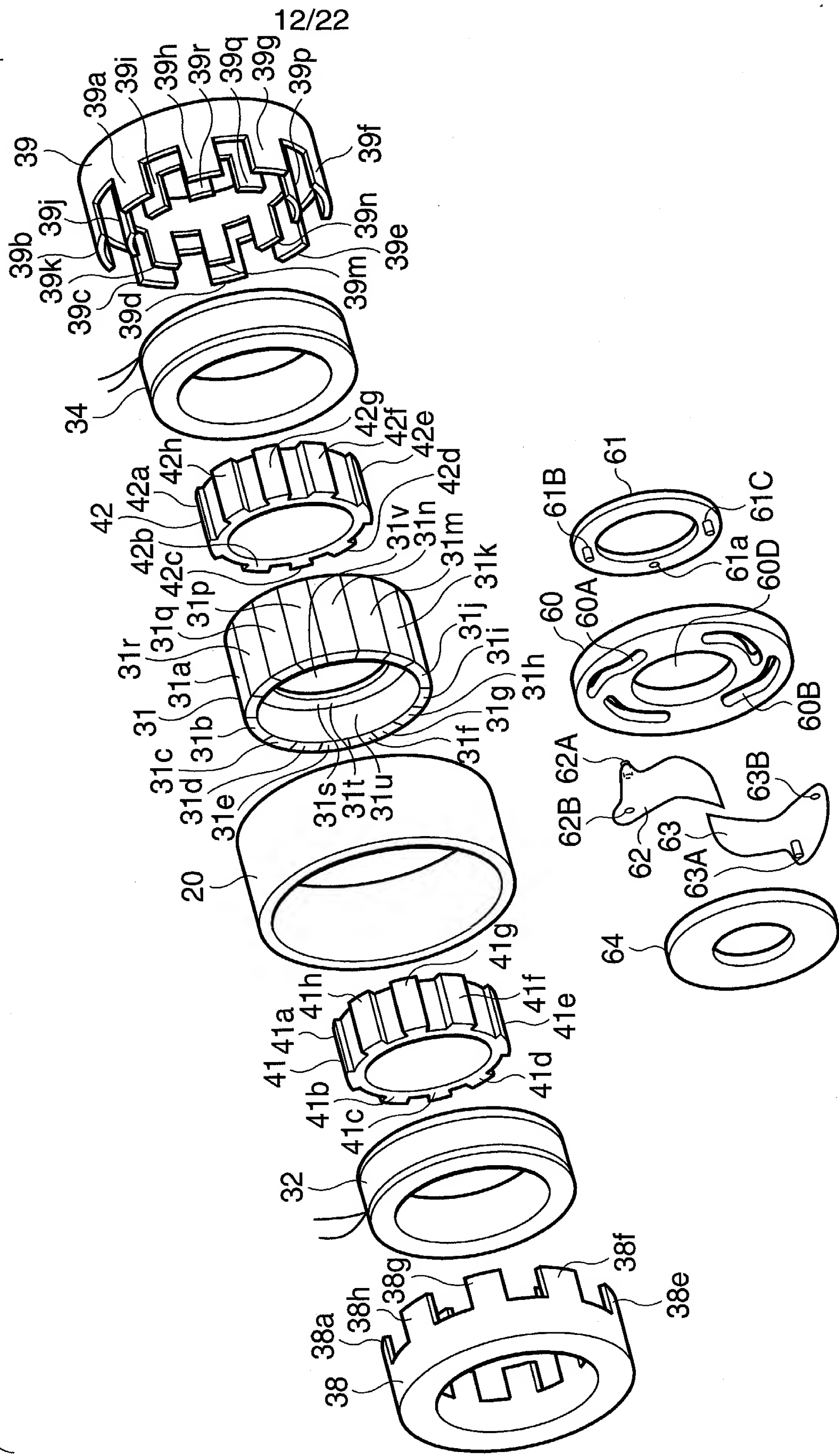


FIG.13

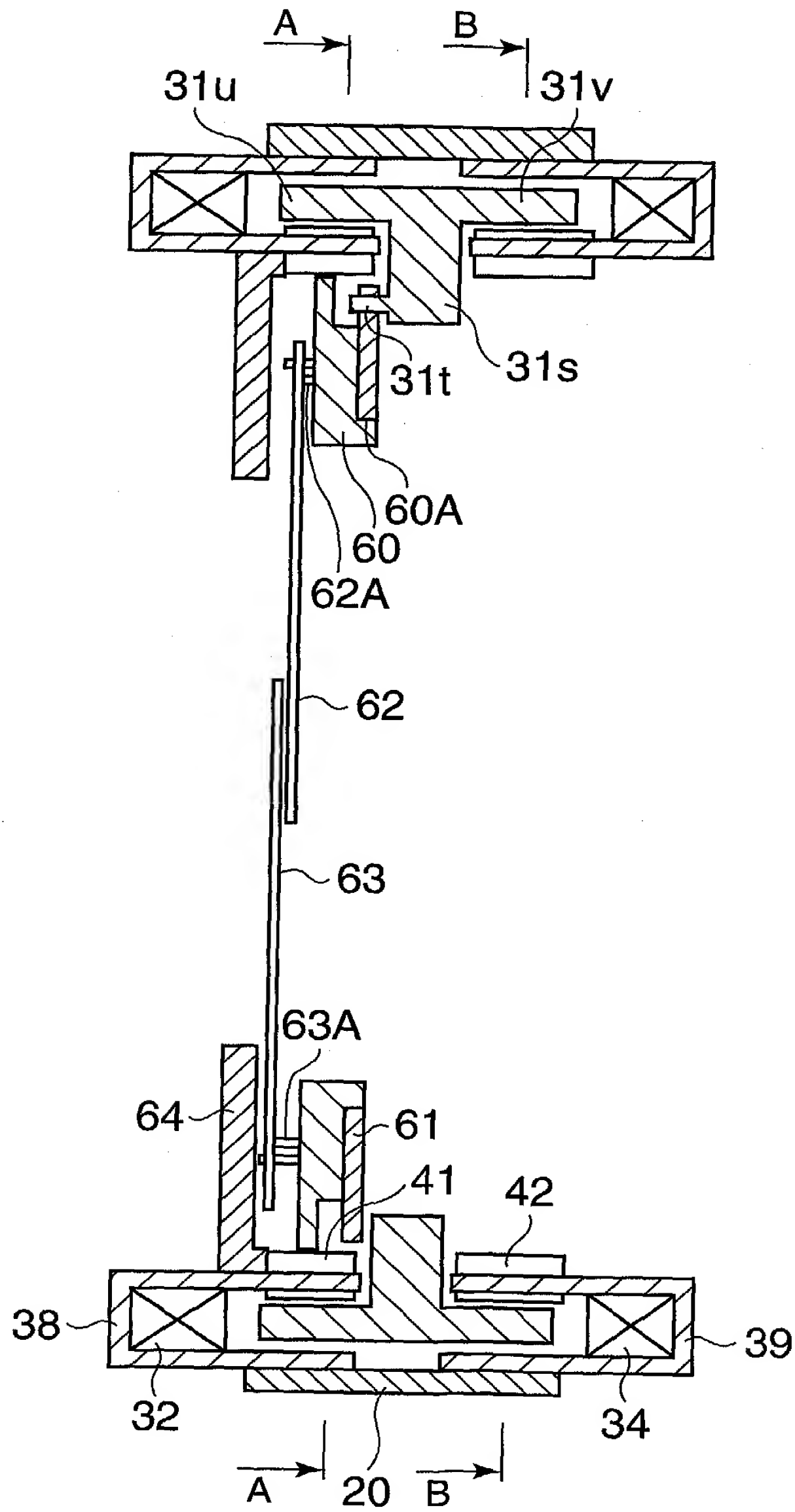


FIG.14A

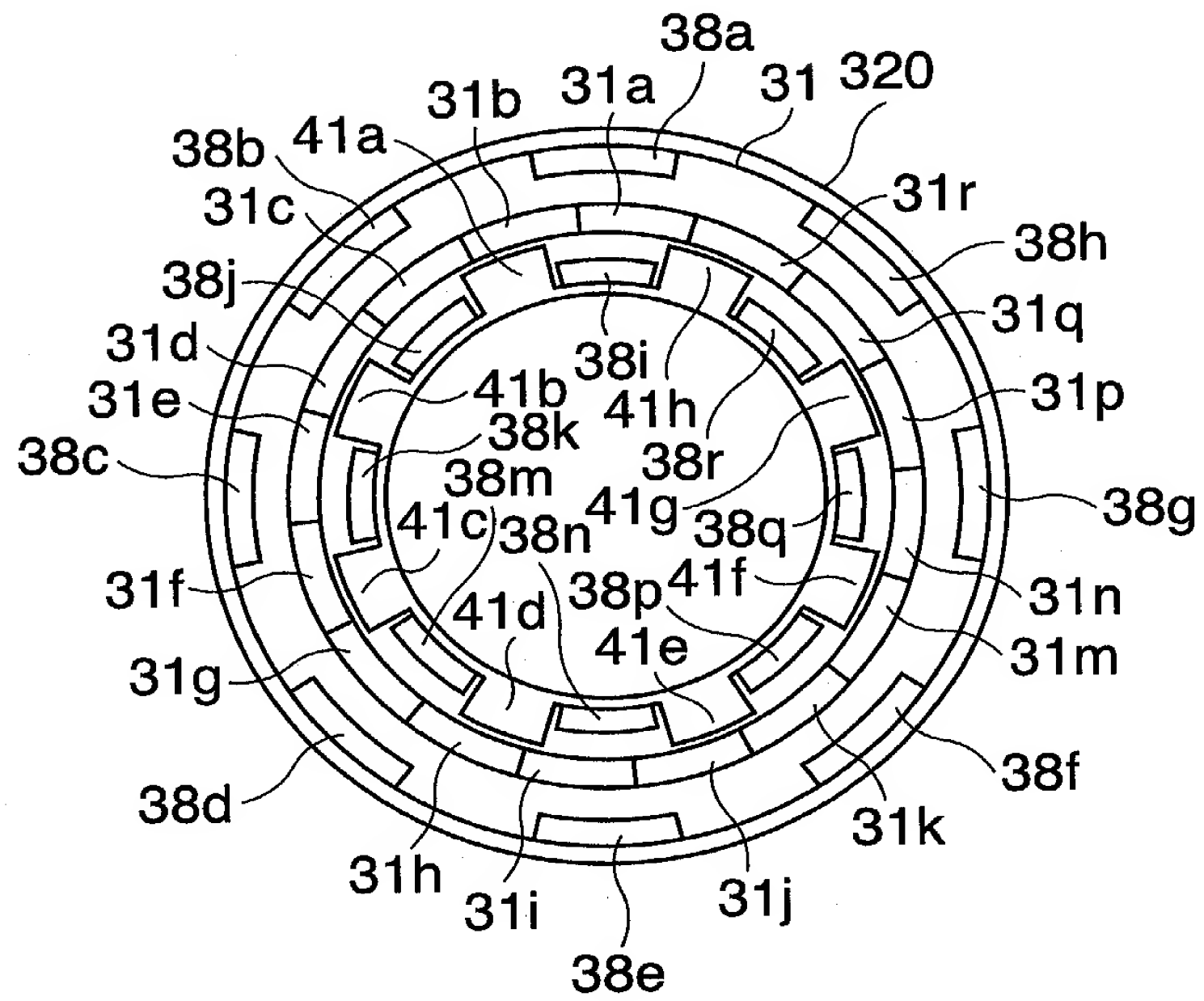


FIG.14B

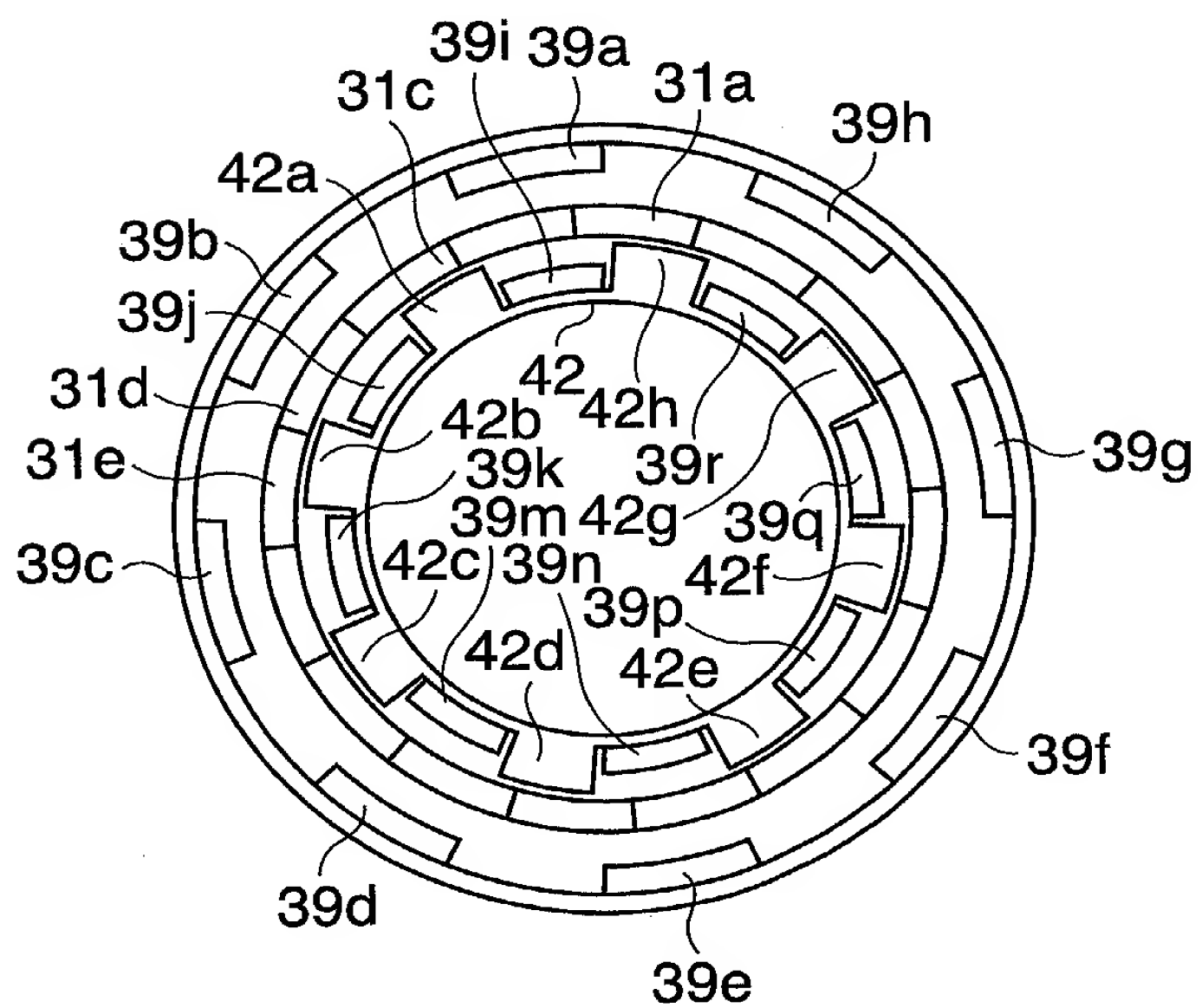


FIG.15

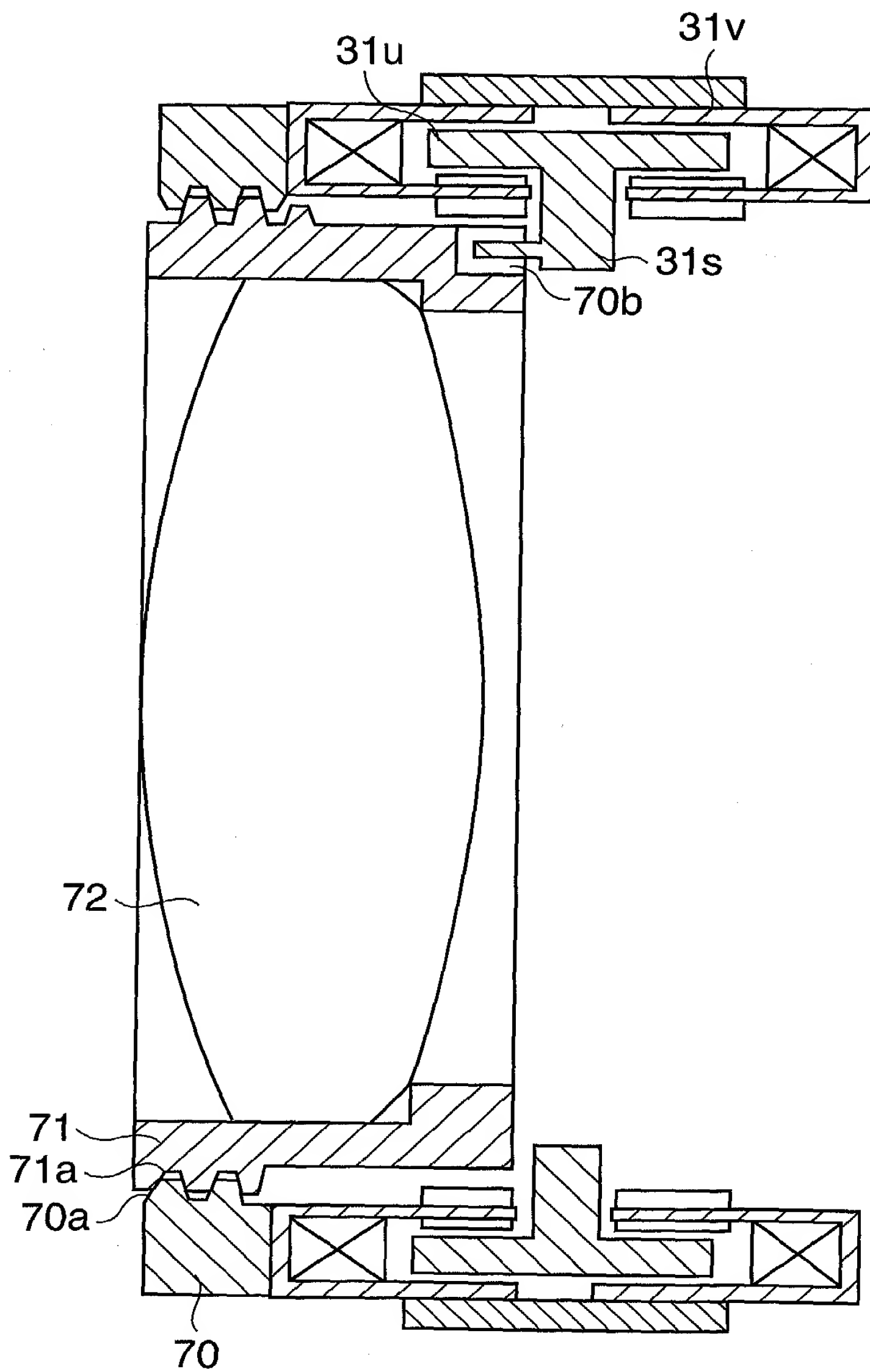


FIG. 15

FIG. 16

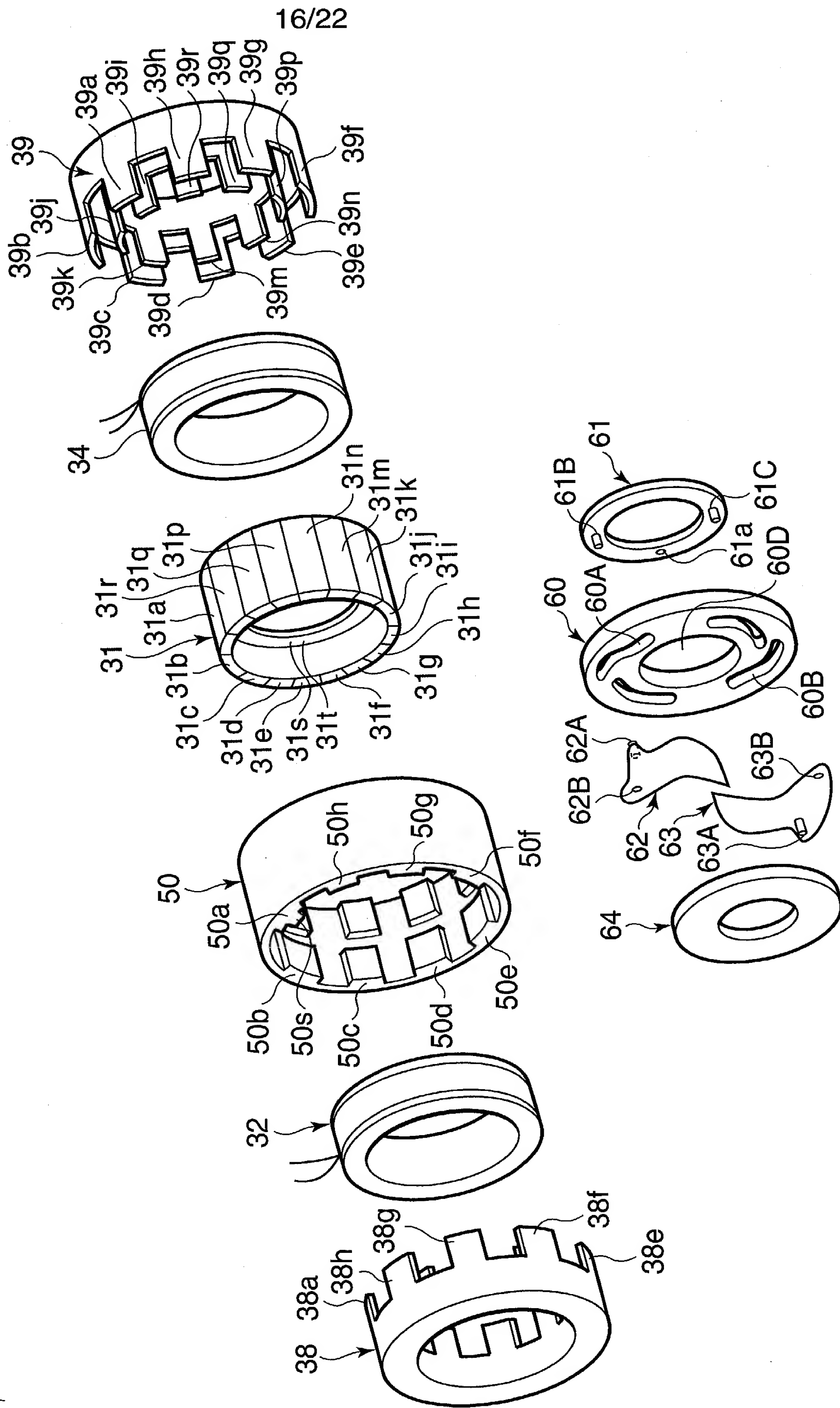




FIG. 1 is a cross-sectional view of a semiconductor device. The device has a central vertical channel (60) containing a series of stacked layers (60A, 62A, 62, 63, 63A) and a central core (64). The channel is flanked by side walls (31, 31s, 31t). The top and bottom of the device are sealed with a cap (38) and a base (39). Various contact pads and regions are labeled, including 50s, 50a, 50i, 50t, 50e, and 50m. Arrows A and B indicate specific directions or planes of interest.

FIG.18A

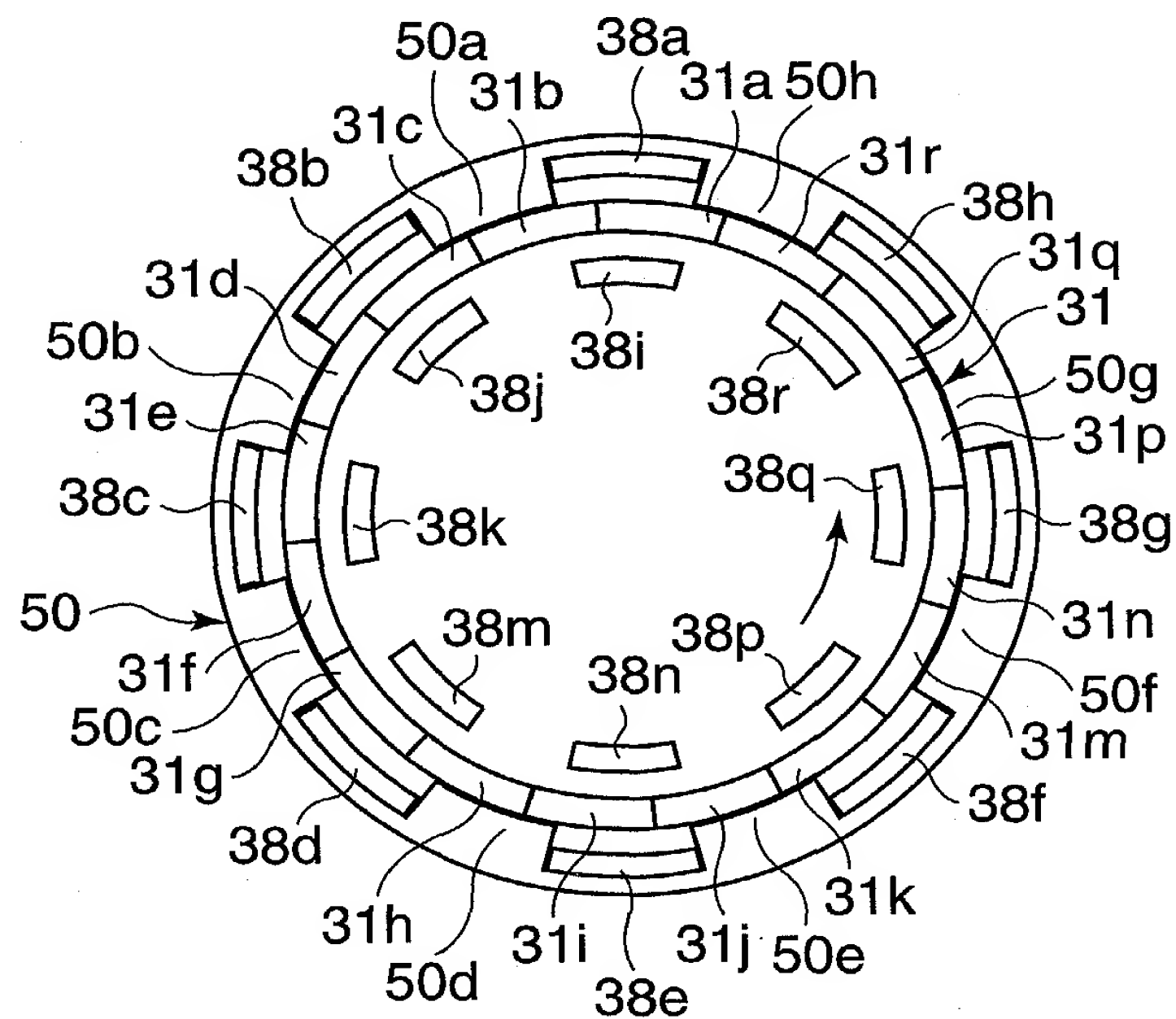


FIG.18B

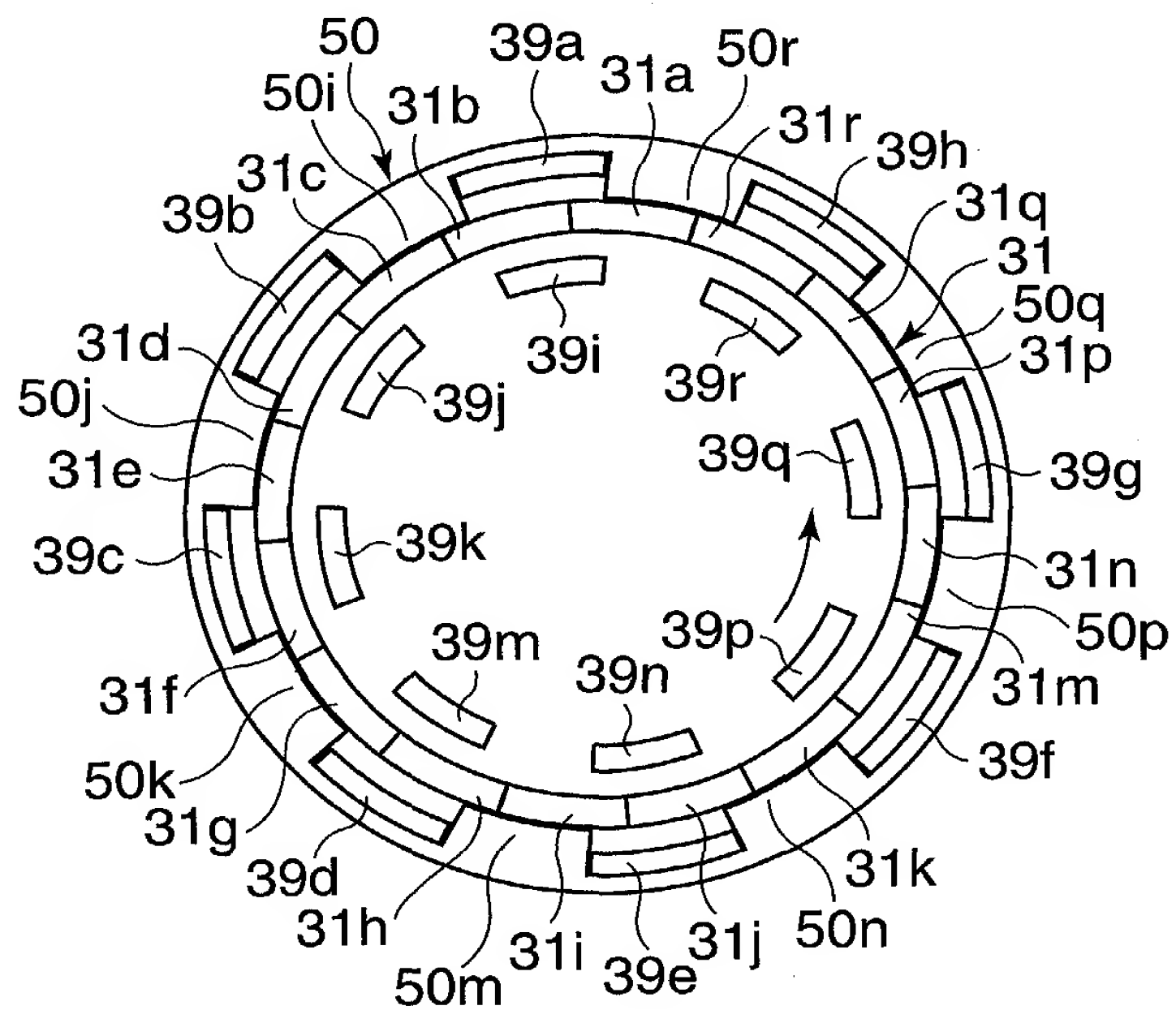


FIG.19

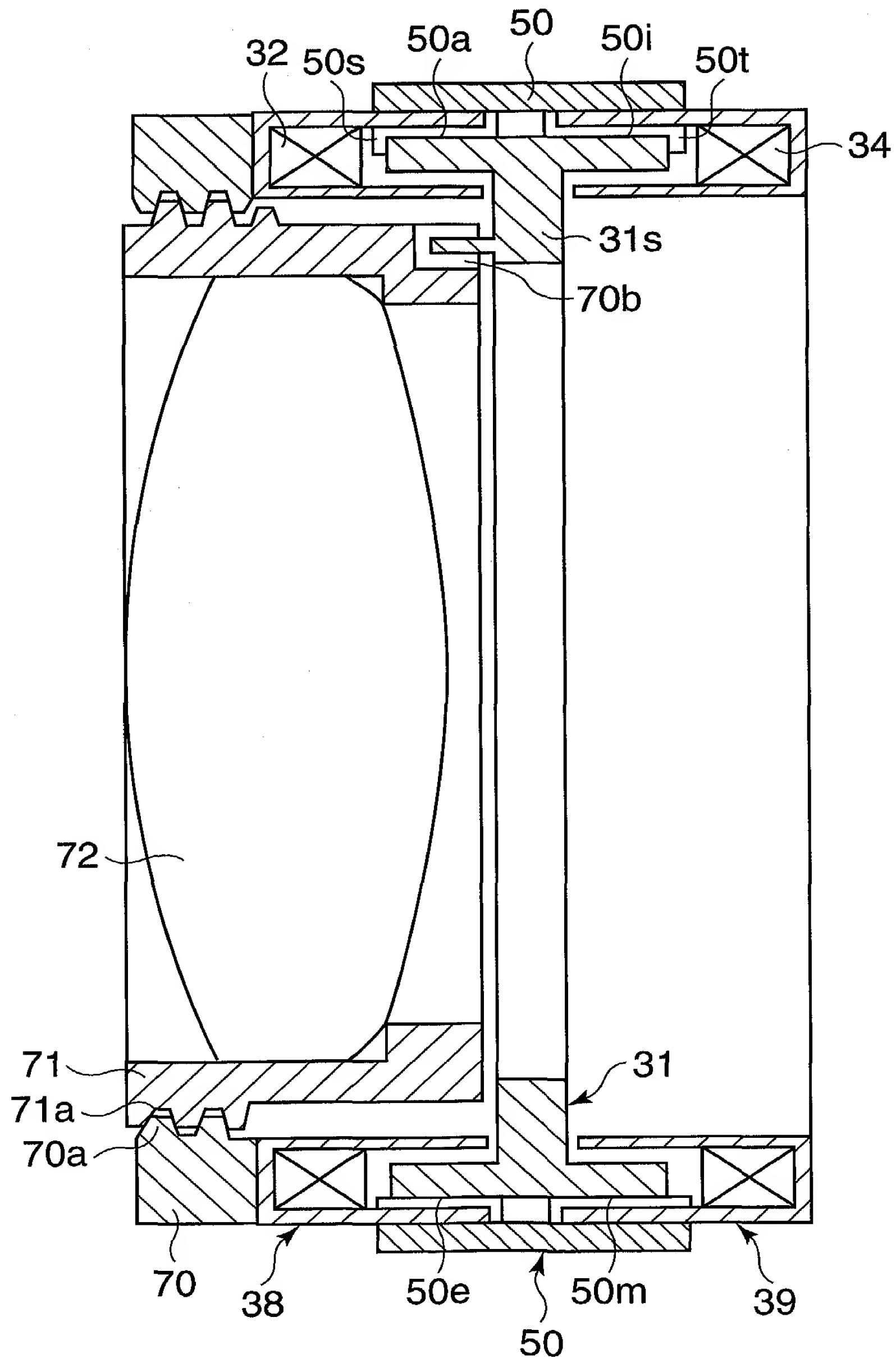


FIG.20

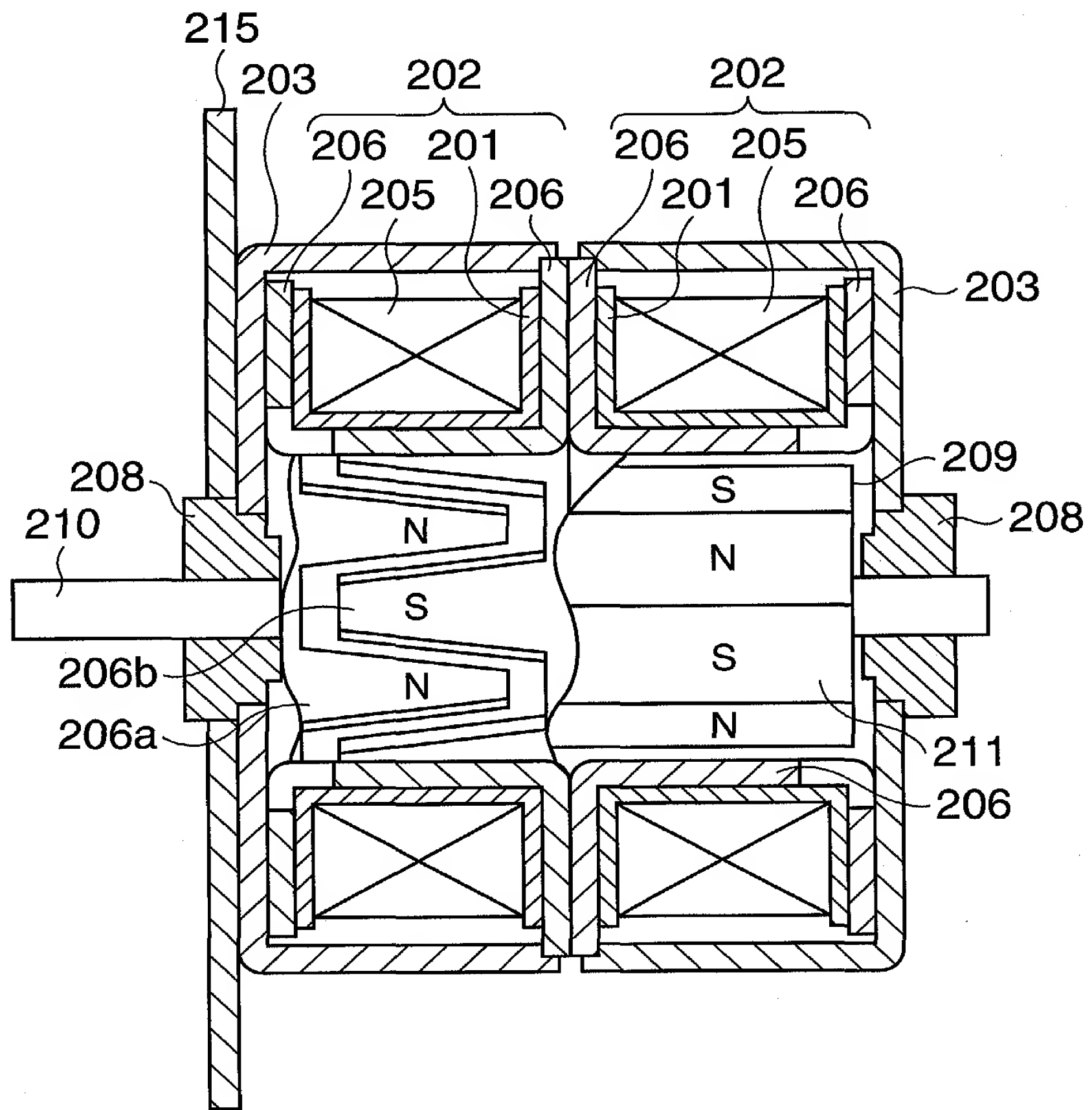
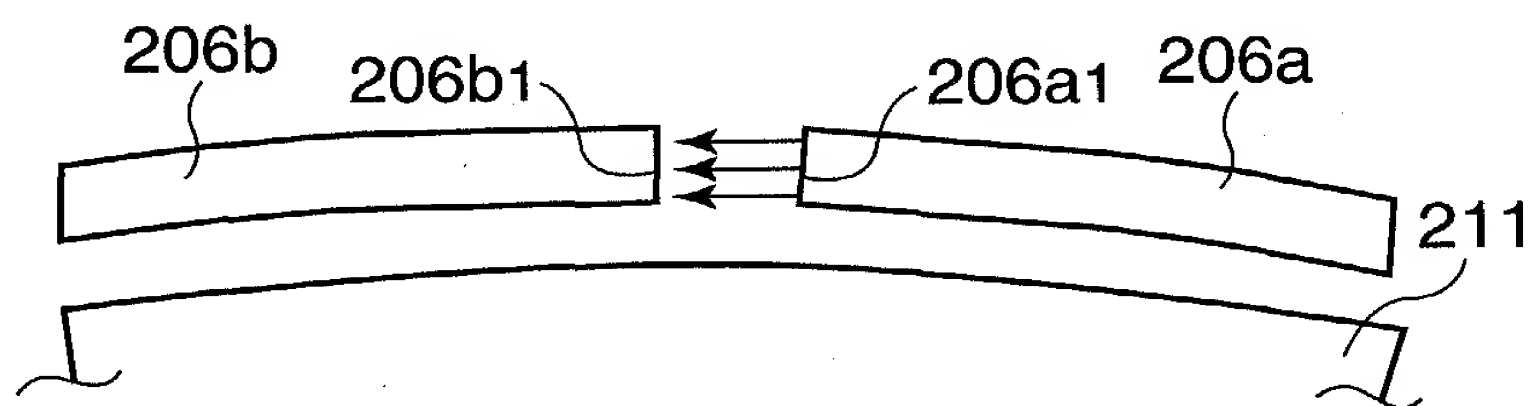


FIG.21



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FIG.22

